

## Ddr3 Layout Guidelines

**Design of DDR3 SDRAM Test Module** Sirisha Prayaga 2007

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*Development of Circuit Layout Guidelines to Prevent CMOS Latchup by Two-dimensional Analysis* Songmin Kim 1990

*Asia Electronics Industry* 2003

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**CMOS IC Layout** Dan Clein 1999-01-07 This book includes basic methodologies, review of basic electrical rules and how they apply, design rules, IC planning, detailed checklists for design review, specific layout design flows, specialized block design, interconnect design, and also additional information on design limitations due to production requirements.\*Practical, hands-on approach to CMOS layout theory and design\*Offers engineers and technicians the training materials they need to stay current in circuit design technology.\*Covers manufacturing processes and their effect on layout and design decisions

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